Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-34 (cancelled).

35 (currently amended): A chip-packaging with bonding options connected to a package substrate, comprising:

the package substrate connected to either a high voltage or a low voltage;

a chip mounted on the package substrate, the chip comprising a plurality of bonding option units, each bonding option unit comprising a bonding pad; and

a plurality of first lead frames, ~~each~~ the bonding pad of each bonding option unit ~~the chip~~ having a corresponding first lead frame, the first lead frames being connected to a voltage logically opposite of the voltage level of the package substrate;

wherein each bonding pad is connected to one of the package substrate and the corresponding first lead frame with the other of the package substrate and the corresponding first lead frame remaining unconnected, thereby providing two types of bonding options for each bonding pad,

wherein the connection of the bonding pad is determined according to the functionality of the chip.

36 (currently amended): A method of packaging two identical chips to two different ICs, comprising:

providing two identical package substrates respectively for the two chips;

respectively mounting each chip on its respective package substrate, each chip comprising a plurality of bonding option units, each bonding option unit comprising a bonding pad;

providing a plurality of first lead frames for each package substrate, ~~each~~ the

bonding pad of each ~~chip~~ bonding option unit having a corresponding first lead frame;

for a said chip, connecting at least one predetermined bonding pad of the said bonding pads to the corresponding package substrate; and

for the other said chip, connecting at least one bonding pad equivalent to the said at least one predetermined bonding ~~pads~~ pad to [[a]] the corresponding first lead frame ~~of the corresponding package substrate~~ such that identical chips are packaged to different ICs.

37 (new): A method of packaging a chip having a bonding option connected to a package substrate, comprising:

providing the package substrate;

connecting the package substrate to either a high voltage or a low voltage;

mounting the chip on the package substrate, the chip comprising a plurality of bonding option units, each bonding option unit comprising a bonding pad;

providing a plurality of first lead frames, the first lead frames being connected to either a high voltage or a low voltage, wherein the voltage level of the first lead frames is the logical opposite of the voltage level of the package substrate; and

determining a connection of the bonding pad of each bonding option unit according to the functionality of the chip.

38 (new): The method of claim 37, further comprising providing the connection by connecting the bonding pad to the package substrate for enabling or disabling the functionality of the chip in different applications.

39 (new): The method of claim 37, further comprising providing the connection by connecting the bonding pad of each bonding option unit to the first lead frame for enabling or disabling the functionality of the chip in different applications.

40 (new): The method of claim 37, further comprising providing a plurality of second lead frames, wherein the second lead frames are used for inputting or outputting signals to the bonding pad.

41 (new): The method of claim 40, further comprising providing the connection by connecting the bonding pad to the second lead frame for enabling or disabling the functionality of the chip in different applications.

42 (new): The method of claim 40, further comprising providing the connection by connecting the bonding pad to the substrate, the first lead frame, or the second lead frame for providing three types of bonding options for each bonding option unit.